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pipelined "virtual router"

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CW Selvidge, A Agarwal, J Babb, ML Dahl - US Patent 5,850,537, 1998 - [freepatentsonline.com](#)

... A row corresponds to a pin and each column to a pipeline clock period ... use count represents the number of channel path conductors used by the virtual router at a ...

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T Spalink, S Karlin, L Peterson, Y Gottlieb - Proceedings of the eighteenth ACM symposium on Operating ..., 2001 - [portal.acm.org](#)

... 3.1 Forwarding Pipeline The common unit of data transferred through the IXP1200 is a 64-byte MAC-Packet (MP). ... Figure 4 summarizes the forwarding pipeline. ...

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GL Steele Jr, WD Hillis, G Blelloch, M Drumbeller, ... - 1989 - [freepatentsonline.com](#)

... 4,773,038; and "Pipelining Technique and Pipelined Processes for Multi-Dimensional Processor ... of the message format supplied to the virtual router in accordance ...

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R Simmonds, R Bradford, B Unger - Parallel and Distributed Simulation, 2000. PADS 2000. ..., 2000 - [ieeexplore.ieee.org](#)

... as, for example, one or more simulated IP packets passes along the pipeline. ... to resolve the (fictitious) IP address and send packets to the virtual router. ...

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### [NetBind: a binding tool for constructing data paths in network processor-based routers](#) - ► [sinica.edu.tw](#) [\[PDF\]](#)

AT Campbell, ST Chou, ME Kounavis, VD Stachos, J ... - Open Architectures and Network Programming Proceedings, 2002 ..., 2002 - [ieeexplore.ieee.org](#)

... A network processor specification augments the virtual router specification with information about the ... A processing pipeline is a set of components that are ...

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### [A fast, simple router for the Data-Intensive Architecture \(DIVA\) system](#) -

► [hmc.edu](#) [\[PDF\]](#)

CW Kang, J Draper - Circuits and Systems, 2000. Proceedings of the 43rd IEEE ..., 2000 - [ieeexplore.ieee.org](#)

... Each virtual router contains controlling logic, consisting of an input controller,

switch, and output con ... 5] Mike Galles, "Scalable Pipelined Interconnect for ...

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## Performance Evaluation of VCRI. Sc: a Virtual Router for Transputer Networks

JP KTTAJ1MA, B PLATEAU - Transputers'92: Advanced Research and Industrial ..., 1992 - books.google.com

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Z Hussain, S Desai, N Alam, J Cheng, T Millet - US Patent App. 10/163,162, 2002 - Google Patents

... 5/6 SEND PACKET TO NEXT PIPELINE STAGE s Page 7. US 2003/0223361 A1 Dec. 4, 2003

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## Method and apparatus for multi-redundant router protocol support

TS Michels, D Clear, J Cathey - EP Patent 1,158,725, 2001 - freepatentsonline.com

... virtual router groups and more than four VRRP virtual router groups simultaneously ... the application engine 206 preferably has a pipelined architecture wherein ...

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►ucalgary.ca [PDF]

C Williamson, R Simmonds, M Arlitt - Performance Evaluation, 2002 - Elsevier

... the interface in promiscuous mode is that a virtual router address and ... connection, either serially (persistent connection) or in a pipelined fashion (pipelined ...

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FH Bennett III, JR Koza, J Shipman, O Stiffelman - Proceedings of the Genetic and Evolutionary Computation ..., 1999 - genetic-programming.com

... The Parsytec virtual router creates a toroidal mesh among the 64 processing nodes. ...

The instruction units are pipelined and able to produce a result on every ...

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## APAP I/O programmable router

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... method thereof. 4984237, January, 1991, Franaszek, 370/388, Multistage network

with distributed pipelined control. 4985832, January, 1991, ...

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... solution would provide the necessary properties, but nothing in the pipeline offers an ... and treated as if it resides entirely within a virtual router defined by ...

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... But nothing in the pipeline offers an easy answer for other noninterference goals ... and treated as if it resides entirely within a virtual router defined by the ...

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... of transputer links for reconfiguration control than in the pipeline-based system ...

Plateau, Performance Evaluation of VCR 1.8 c: a Virtual Router for Transputer ...

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### Advanced parallel array processor (APAP)

TN Barker, CA Collins, MC Dapp, JW Dieffenderfer, ... - US Patent 5,717,943, 1998 - freepatentsonline.com

... and wherein an array of nodes is provided with means for directed inter-processor memory element communication for preparing data for pipelined very high speed ...

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